AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (withdrawn) An integrated circuit package, comprising:

a) a die pad having a first face and a second face opposite to said first face;

b) a plurality of inner leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of inner leads is disposed substantially co-planar with and substantially around said die pad;

c) a plurality of outer leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of outer leads is disposed substantially co-planar with and substantially around said plurality of inner leads and said die pad, such that said sides of each of said plurality of outer leads are substantially offset from said sides of each of said plurality of inner leads;

d) a first adhesive layer disposed on said first face of said die pad;

e) a second adhesive layer disposed on said first face of said plurality of inner leads;

f) an integrated circuit chip having a first face and a second face opposite to said first face,

wherein said second face of said integrated circuit chip is coupled to said first face of said die pad through said first adhesive layer, and

wherein said second face of said integrated circuit chip is further coupled to said first face of said plurality of inner leads through said second adhesive layer;

g) a first plurality of wires linking said plurality of inner leads to said integrated circuit chip, each of said first plurality of wires comprising:

a first end electrically conductively joined to said first face of one of said plurality of inner leads, and

a second end electrically conductively joined to said first face of said integrated circuit chip; and

h) a second plurality of wires linking said plurality of outer leads to said integrated circuit chip, each of said second plurality of wires comprising:

a first end electrically conductively joined to said first face of one of said plurality of outer leads, and

a second end electrically conductively joined to said first face of said integrated circuit chip.

2. (withdrawn) The integrated circuit package according to claim 1, further comprising:

i) an encapsulant surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive layer, said second adhesive layer, said first plurality of wires, said second plurality of wires, and said integrated circuit chip.

3. (withdrawn) The integrated circuit package according to claim 2, wherein said encapsulant is a polymer-based molding compound.

4. (withdrawn) The integrated circuit package according to claim 1, wherein said die pad, said plurality of inner leads, and said plurality of outer leads are composed of a common copper alloy.

5. (withdrawn) The integrated circuit package according to claim 1, wherein said first plurality of wires and said second plurality of wires are composed of one of a group comprising: gold, gold with some level of impurities, aluminum, and copper.

6. (withdrawn) The integrated circuit package according to claim 1, further comprising:

i) a conductive element having a first face and a second face opposite to said first face, wherein said conductive element is sandwiched between said die pad and said integrated circuit chip,

such that said second face of said conductive element is coupled to said first face of said die pad through said first adhesive layer;

said second face of said conductive element is further coupled to said first faces of said plurality of inner leads through said second adhesive layer, and

said first face of said conductive element is coupled to said second face of said integrated circuit chip through a third adhesive layer;

j) at least one first linking wire linking said integrated circuit chip to said conductive element, said at least one first linking wire having

a first end electrically conductively joined to said first face of said conductive element, and

a second end electrically conductively joined to said first face of said integrated circuit chip; and

k) at least one second linking wire linking said die pad to said conductive element, said at least one second linking wire having

a first end electrically conductively joined to said first face of said conductive element, and

a second end electrically conductively joined to said first face of said die pad.

7. (withdrawn) The integrated circuit package according to claim 6, wherein said second plurality of wires, said at least one first linking wire and said at least one second linking wire are composed of one of a group comprising: gold, gold with some level of impurities, aluminum, and copper.

8. (withdrawn) The integrated circuit package according to claim 6, further comprising:

l) an encapsulant surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive, said second adhesive, said conductive element, said third adhesive, said IC chip, said first plurality of wires, said second plurality of wires, said first linking wire, and said second linking wire.

9. (withdrawn) The integrated circuit package according to claim 8 wherein said encapsulant is a polymer-based molding compound.

10. (withdrawn) An integrated circuit package, comprising:

a) a die pad having a first face and a second face opposite to said first face;

b) a plurality of inner leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of inner leads is disposed substantially co-planar with and substantially around said die pad;

c) a plurality of outer leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of outer leads is disposed substantially co-planar with and substantially around said plurality of inner leads and said die pad, such that said sides of each of said plurality of outer leads are substantially offset from said sides of each of said plurality of inner leads;

d) a first adhesive layer disposed on said first face of said die pad;

e) a second adhesive layer disposed on said first face of said plurality of inner leads;

f) a first integrated circuit chip having a first face and a second face opposite to said first face,

wherein said section face of said first integrated circuit chip is coupled to said first face of said die pad through said first adhesive layer, and

wherein said second face of said first integrated circuit chip is further coupled to said first face of said plurality of inner leads through said second adhesive layer;

g) a third adhesive layer disposed on said first face of said first integrated circuit chip;

h) a second integrated circuit chip having a first face and a second face opposite to said first face,

wherein said second face of said second integrated circuit chip is coupled to said first face of said first integrated circuit chip through said third adhesive layer;

i) a first plurality of wires linking said plurality of inner leads to said first integrated circuit chip, each of said first plurality of wires comprising:

a first end electrically conductively joined to said first face of one of said plurality of inner leads, and

a second end electrically conductively joined to said first face of said first integrated circuit chip; and

j) a second plurality of wires linking said plurality of outer leads to said second integrated circuit chip, each of said second plurality of wires comprising:

a first end electrically conductively joined to said first face of one of said plurality of outer leads, and

a second end electrically conductively joined to said first face of said second integrated circuit chip.

11. (withdrawn) The integrated circuit chip according to claim 10, further comprising:

k) an encapsulant surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive layer, said second adhesive layer, said first integrated circuit chip, said third adhesive layer, said second integrated circuit chip, said first plurality of wires, and said second plurality of wires.

12. (withdrawn) The integrated circuit package according to claim 11, wherein said encapsulant is a polymer-based molding compound.

13. (withdrawn) The integrated circuit package according to claim 10, wherein said die pad, said plurality of inner leads, and said plurality of outer leads are composed of a common copper alloy.

14. (withdrawn) The integrated circuit package according to claim 10, wherein said plurality of wires is composed of one of a group comprising: gold, gold with some level of impurities, aluminum, and copper.

15. (withdrawn) A leadframe for an integrated circuit package, comprising:

a) an outer frame portion;

b) a die pad portion substantially centrally disposed within said outer frame portion;

c) a plurality of inner lead portions extending substantially radially outward from said central die pad portion;

d) a plurality of outer lead portions extending substantially radially inward from said outer frame portion; and

e) a plurality of tie bars connecting said die pad portion to said outer frame portion.

16. (withdrawn) The leadframe according to claim 15, having a first face and a second face, wherein

a dimple is formed on the first face of each of said plurality of inner lead portions, and

a plurality of dimples are formed on the first face of said die pad portion.

17. (withdrawn) The leadframe according to claim 15, wherein the leadframe is composed of a common copper alloy.

18. (withdrawn) A leadframe for an integrated circuit package, comprising:

a) an outer frame portion;

b) a die pad portion substantially centrally disposed within said outer frame portion;

c) a plurality of tie bars connecting said die pad portion to said outer frame portion;

d) a plurality of protuberances extending substantially radially inward from said outer frame portion, each of said plurality of protuberances comprising:

an inner lead portion,

an outer lead portion, and

a post portion connecting said inner lead portion to said outer lead portion, said post portion having a substantially smaller width than either said inner lead portion or said outer lead portion.

19. (withdrawn) The leadframe according to claim 18, having a first face and a second face, wherein

a dimple is formed on the first face of each of said plurality of inner lead portions, and

a plurality of dimples are formed on the first face of said die pad portion.

20. (withdrawn) The leadframe according to claim 18, wherein the leadframe is composed of a common copper alloy.

21. (original) A method of assembling an integrated circuit package, comprising:

a) providing:

a die pad having a first face and a second face opposite to said first face,

a plurality of inner leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face,

a plurality of outer leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face,

an integrated circuit chip having a first face and a second face opposite to said first face, and

a conductive element having a first face and a second face opposite to said first face;

b) disposing said inner leads substantially co-planar with and substantially around said die pad;

c) disposing said outer leads substantially co-planar with and substantially around said inner leads and said die pad, such that said plurality of sides of said plurality of outer leads is offset from said plurality of sides of said plurality of inner leads;

d) coupling said second face of said conductive element to said first face of said die pad through a first adhesive layer;

e) further coupling said second face of said conductive element to said first faces of said plurality of inner leads through a second adhesive layer;

f) coupling said second face of said integrated circuit chip to said first face of said conductive element through a third adhesive layer;

g) electrically conductively linking each of said plurality of inner leads to said first face of said integrated circuit chip;

h) electrically conductively linking each of said plurality of outer leads to said first face of said integrated circuit chip;

i) electrically conductively linking said first face of said integrated circuit chip to said conductive element; and

j) electrically conductively linking said conductive element to said die pad.

22. (original) The method according to claim 21, further comprising:

k) coupling said second face of said die pad, said second face of each of said plurality of inner leads, and said second face of each of said plurality of outer leads to a printed circuit board through a fourth adhesive layer.

23. (original) The method according to claim 22, wherein said fourth adhesive layer comprises a conductive adhesive film or an electrically conductive paste.

24. (original) A method of assembling an integrated circuit package, comprising:

a) providing:

a leadframe having a first face and a second face opposite to said first face, wherein said leadframe comprises:

an outer frame portion,

a die pad portion substantially centrally disposed within said outer frame portion,

a plurality of inner lead portions extending substantially radially outward from said die pad portion, each of said plurality of inner leads comprising an inner portion, a central portion and an outer portion,

a plurality of outer lead portions extending substantially radially inward from said outer frame portion, and

a plurality of tie bars connecting said die pad portion to said outer frame portion, each of said plurality of tie bars comprising an inner portion and an outer portion,

an integrated circuit chip having a first face and a second face opposite to said first face,

a first plurality of wires each having a first end and a second end, and

a second plurality of wires each having a first end and a second end;

b) disposing an adhesive layer on said first face of said leadframe, whereby said first adhesive layer covers said die pad portion, said inner portion and said central portion of said plurality of inner lead portions, and said inner portion of said plurality of tie bars, and whereby said outer portion of said plurality of inner lead portions remains free of adhesive;

c) severing said outer and central portions of said plurality of inner lead portions from said inner portions of said plurality of inner lead portions and from said die pad portion;

d) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to said first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit chip is further connected to said first faces of said plurality of inner lead portions through said adhesive layer;

e) electrically conductively joining said first end of each of said first plurality of wires to said first face of said outer portion of one of said plurality of inner lead portions;

f) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip;

g) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said plurality of outer leads; and

h) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.

25. (original) A method of assembling an integrated circuit package, comprising:

a) providing:

a leadframe having a first face and a second face opposite to said first face, wherein said leadframe comprises:

an outer frame portion,

a die pad portion substantially centrally disposed within said outer frame portion,

a plurality of tie bars connecting said die pad portion to said outer frame portion, and

a plurality of protuberances extending substantially radially inward from said outer frame portion, each of said plurality of protuberances comprising an inner lead portion, and outer lead portion, and a post portion connecting said inner lead portion from said outer lead portion,

an integrated circuit chip having a first face and a second face opposite to said first face,

a first plurality of wires each having a first end and a second end, and

a second plurality of wires each having a first end and a second end;

b) disposing an adhesive layer on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead portion of each of said plurality of protuberances, wherein part of each of said inner lead portions remains free of adhesive;

c) severing said outer lead portion from said inner lead portion by cutting said post portion;

d) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to said first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer;

e) electrically conductively joining said first end of said first plurality of wires to said first face of one of said plurality of inner lead portions;

f) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip;

g) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said outer lead portions, and

h) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.

26. (original) The method according to claim 25, wherein the adhesive layer disposed on said first face of said lead frame in step (b) covers only an outer edge of said die pad portion, and part of said outer lead portion of each of said plurality of protuberances, thereby leaving a

central part of said die pad portion and a part of each of said outer lead portions remains free of adhesive.

27. (new) A method of assembling an integrated circuit package, comprising:

a) providing:

a leadframe having a first face and a second face opposite to said first face, wherein said leadframe comprises:

an outer frame portion,

a die pad portion substantially centrally disposed within said outer frame portion,

a plurality of tie bars connecting said die pad portion to said outer frame portion, and

a plurality of protuberances extending from said leadframe, wherein some of said protuberances comprise at least a plurality of inner lead portions and some of said protuberances comprise at least a plurality of outer lead portions;

an integrated circuit chip having a first face and a second face opposite to said first face,

a first plurality of wires each having a first end and a second end, and

a second plurality of wires each having a first end and a second end;

b) disposing an adhesive layer on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead portions, wherein part of each of said inner lead portions remains free of adhesive;

c) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to said first face of said die pad portion through said

adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer;

d) electrically conductively joining said first end of said first plurality of wires to said first face of one of said plurality of inner lead portions;

e) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip;

f) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said outer lead portions, and

g) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.